Optical Interconnects for Future Advanced Antenna Systems: Architectures, Requirements and Technologies

Francesco Testa, Mark T. Wade, Mikael Lostedt, Fabio Cavaliere, Marco Romagnoli, Vladimir Stojanović

***Abstract*—This paper aims to give an outlook of future advanced antenna systems for 5G and 6G wireless networks. The trend to increase the peak data rate and to reduce latency and power consumption will continue in the future. This will be made possible by the exploitation of millimeter wave frequency bands and by the introduction of massive multiple-input multiple-output antenna technology which requires a transformation of the antenna hardware architectures and technologies. Advanced antenna systems based on arrays of several hundreds of antenna elements are under development and to keep the fronthaul throughput manageable, some digital signal processing functions have been moved inside the antenna, creating the need to distribute very big volumes of data at high bit rate across the antenna. The characteristics and hardware architecture of future advanced antenna systems are discussed and the relevant interconnect requirements are presented.**

A new type of monolithically integrated optical transceiver is presented, integrating electronic and photonic circuits on the same chip with high bandwidth density, high energy efficiency and low latency. The transceiver technology is discussed and results of experimental demonstrations are given.

***Index Terms*—Antenna arrays, Optical transmitters, Optical receiver, MIMO, Mobile communication, Silicon Photonics, Optical interconnects**

I. Introduction

OPTICAL technologies have been extensively used in 4G radio access networks to interconnect, in a split radio base station (RBS), the baseband unit (BBU), e.g. placed at a basement or at the roof of a building, to the remote radio unit (RU), typically placed at few hundred meters distance on top of a pole or cell tower. Optical systems have become the traditional communication technology for this network segment named 'fronthaul'. The moderate fronthaul data throughput for interconnecting a single BBU to a number of RUs, of the order of 100 Gbps, favoured the use of commercial pluggable modules as optical transceivers. In the evolution from the beginning of 4G era to 5G wireless systems, a new radio (NR) access technology has been developed [1], [2], [3] to address a variety of usage scenarios from enhanced mobile broadband to ultra-reliable low-latency communications to massive machine- type communications and new performance targets have been set: peak data rate has to be increased from 100 Mbps up to 10 Gbps, minimum latency has to be decreased down to 1 ms for certain time-sensitive applications, mobile data volume per geographical area will be expanded by a factor of 1000 and energy efficiency per transported bit will be increased by a factor of 10 [4], [12]. To fulfill these challenging requirements RF carriers in the millimeter-wave (mmW) range will be exploited to allow the radio channel bandwidth expansion from 20 MHz to up to 1 GHz, together with advanced technologies for increasing radio performances like beamforming and massive multiple-input multiple-output (m-MIMO) [5]. This has led to a significant transformation of the antenna systems with an increase in the number of antenna elements from a low count in LTE (e.g., 2x2 or 4x4) to several hundred in mmW advanced antenna systems (AAS).

In 6G systems this trend is expected to continue with a further increase in the peak data rate up to 100 Gbps, thanks to the exploitation of ultra-massive MIMO and the use of higher carrier frequency in the Terahertz band (100-1000 GHz) [6].

In this scenario, a radical architectural change in the RU implementation occurs: the antennas for 5G and 6G will be no longer simply converting digital antenna samples received by the BBU into RF signals to be transmitted over the air, but they include several digital processing functions (previously resident in the BBU) to avoid explosion of the bandwidth requirements in the front-haul links [7].

Moving some digital processing functions inside the antenna, mitigates the fronthaul bandwidth requirement but created the need to interconnect a number of digital application specific integrated circuits (ASICs) to many radio frequency integrated circuits (RFICs) distributed across the antenna, close to the antenna elements. In the most extreme scenario, the total throughput can be several Terabit/s.

Key enablers for the evolution of future advanced antenna systems will be the optical interconnect technologies. It becomes indeed impractical to distribute such a huge amount of data at high speed across the antenna via electrical printed circuit board (PCB) lines, due to the high loss and power consumption that increase with the data rate and for the increased signal degradation due to PCB parasitic and electromagnetic interference.

On the other hand, the optical interconnection technologies for radio systems have characteristics different from the silicon

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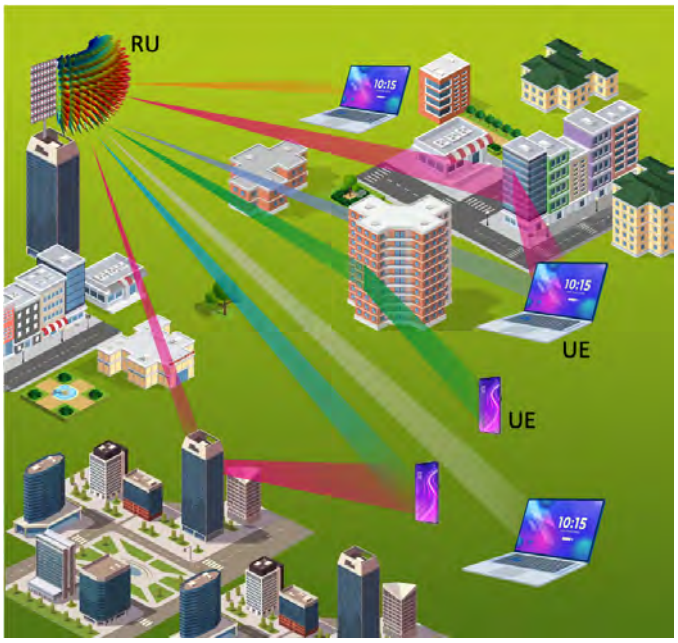


Fig. 1. Beamforming and spatial multiplexing in a massive MIMO system. RU, radio unit; UE, user equipment.

photonics-based interfaces developed for data centers in terms of bandwidth density, bandwidth scalability, energy efficiency, operating temperature range, latency and cost as will be discussed in this paper.

The paper is organized as follows: in Section II future radio systems are introduced together with a short explanation of the technologies used to improve the system performance in terms of data rate, coverage, spectral efficiency and interference management. Section III presents the advanced antenna architectures with focus on the internal interconnect technologies and in section IV the main interconnect requirements are discussed. Section V is dedicated to enabling technologies and the $TeraPHY^{TM}$ chipset is presented and discussed together with some experimental results. Finally, in section VI the perspectives and future research directions are drawn.

II. Future Radio Systems

4G wireless networks are saturating the capacity at lower frequency bands ($<$ 3 GHz), especially in dense urban areas and the continuous growing demand of bandwidth in 5G systems has to be supported by stepping up to higher frequency bands at sub-6GHz (also called mid-band) and at mmW (also called high-band). Here more bandwidth is available and transmission time (and latency) are lower.

Increasing the carrier frequency, the signal on air suffers from a stronger attenuation and is subject to strong absorptions when hitting objects; after few reflections the signal is completely absorbed.

Beamforming is a technique in which different versions of the same signal are transmitted over N antenna elements, each with a controlled phase and amplitude such that the different contributions add constructively at the particular location of the receiver antenna with the amplitude of the resulting waves being N times higher than the amplitude transmitted by a single element [8]. By adopting the beamforming technique, many narrow beams can be created by a large antenna array and directed toward many user equipments, increasing the signal quality (see Fig. 1).

With beamforming, it is then possible to compensate for the loss at higher frequency and provide both an improved coverage and a higher capacity. A massive MIMO (m-MIMO) system is an advanced antenna comprising a very large number of antenna elements and exploiting beamforming [9], [10]. In addition to transmitting many beams toward many different user equipments, with beamforming it is also possible to use multiple antenna elements to transmit simultaneously multiple beams to the same receiving equipment through different propagation paths, each beam carrying different data. This technique is named spatial multiplexing and it allows to further increase the bandwidth. Beamforming is also beneficial to reduce the interference since the energy associated with each beam is spatially confined and directed toward a specific user. In addition, also the spectral efficiency can be maximized since the same time-frequency resources can be re-used in the different beams.

In a typical beamforming system, the antenna array consists of a square matrix of antenna elements. A higher number of antenna elements gives a more focused beam and a higher antenna gain which leads to increased capacity and coverage. Since the size of the antenna is inversely proportional to the frequency, if antenna arrays with hundreds of elements are feasible in the mid-band, this number increases to a few thousands in high-band and to several thousands in the THz band (0.1-1 THz) for 6G wireless systems as consequence of the sub-millimeter reduction of the antenna element pitch.

One of the most relevant aspects of future radio systems is the type of implementation used for beamforming. There are two different implementations: digital and analog beamforming, very different in characteristics and performances [11]. A combination of them, called hybrid beamforming, is also possible.

In an analog beamforming TX (see Fig. 2a), there is one digital signal source whose data are converted by a digital to analog (D/A) converter into an analog signal (if it is an IF signal it is also frequency upconverted by a mixer) and split into N copies, being N the number of antenna elements contributing to the beamforming. Each copy of the signal is appropriately phase shifted in order to generate a highly directional beam. Finally, the various output signals are power amplified and sent over the air. Beamforming can be implemented also at the receiver where the various components of the beam are detected, low-noise amplified in the front-end, individually delayed and combined before the analog to digital (A/D) converter (see Fig. 2b).

In a digital beamforming TX (see Fig. 3a), many digital streams are generated and time shifted by a digital processor, each of them is D/A converted, amplified and sent over the air. In the receiver direction of a digital beamforming system (see Fig. 3b), these functions are simply inverted. The advantages of analog beamforming rely on the limited volume of digital data exchanged between digital processor

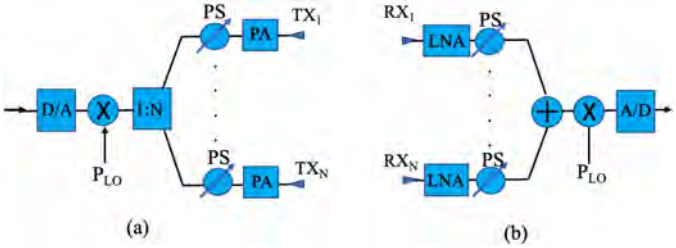


Fig. 2. Analog Beamforming: (a) TX and (b) RX architecture. PA, power amplifier; LNA, low noise amplifier; PS, phase shifter; D/A, digital to analog converter; A/D, analog to digital.

and the front-end requiring processor with less computation power and the use of a single D/A converter featuring low power consumption. However, the system performance is also limited since this type of antenna can only transmit one beam at a given time and it is not suitable for massive MIMO where many focused beams have to be directed toward many user terminals. This drawback can be mitigated with hybrid beamforming solutions using a few digital signal sources. At each source analog beamforming is applied to generate a number of delayed signal copies distributed across a number of antenna elements. With this technique, it is possible to generate a limited number of beams. In fully digital beamforming instead, each antenna element receives its individual digital stream from the beamforming digital processor with phase shifts simultaneously controlled for different sub-bands within the same OFDM symbol. This gives the maximum flexibility in handling the radio time-frequency-space resources and in generating a number of superimposed beams to adapt to multi-path and frequency-selective fading. This allows to optimize spectral efficiency, capacity, signal quality and to increase the number of connected radio equipment.

The drawbacks of digital beamforming are the required digital processor complexity and its power consumption but especially the needed interconnect bandwidth, that can reach several Terabit/s as it will be explained in the following section. The development of high bandwidth density optical interconnects featuring low power, low latency and low cost is of paramount importance to overcome the interconnect bandwidth bottleneck in advanced antenna systems.

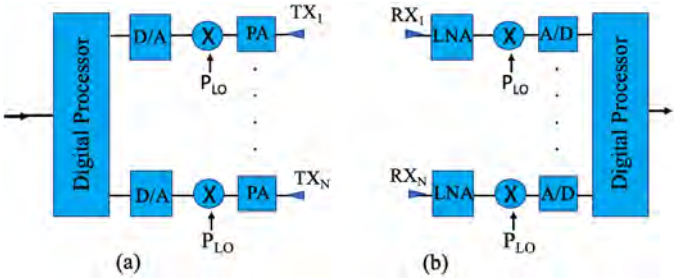


Fig. 3. Digital Beamforming: (a) TX and (b) RX architecture. PA, power amplifier; LNA, low noise amplifier; PS, phase shifter; D/A, digital to analog converter; A/D, analog to digital converter.

III. ADVANCED ANTENNA ARCHITECTURE

As explained above, the advanced antenna systems are undergoing a significant architectural transformation that will require soon the introduction of new hardware technologies to avoid interconnect bottlenecks. In this section an outlook of the new functionalities of the advanced antenna is given and the new antenna architecture is discussed.

To understand the interconnect bandwidth requirements in the new antennas the distribution of the processing functions of the physical layer of Radio systems in the different hardware units (e.g. the BBU and the RU) has to be briefly analysed. We have assumed that the exchange of data between the different hardware units of the radio system occurs via digitized optical interfaces. The alternative implementation based on analog optical interfaces transporting RF signals over fibers (RFoF) between the BBU and an 'all analog' RU, has been investigated [12], [15]. This solution presents some advantages in terms of power consumption and low cost of the RU since the signals are transmitted in the RF form and there is no need to digitize them with A/D and D/A converters. These RFoF links require also lower bandwidth since the digitization process of the radio samples increases the bandwidth requirement by a factor equal to the number of bits of the A/D and D/A converters. However, in RFoF there are also fundamental limitations impacting both the system performances and the transmission performances. The non-linear effects in optical modulators are exacerbated by the use of orthogonal frequency division multiplexing signals, which have a high peak- to-average power ratio (PAPR), limiting the link spurious-free dynamic range (SFDR). Additionally, in RFoF it is very difficult to implement a fully digital beamforming radio system. Indeed, all the digital streams are generated in the BBU but then a high number of analog signals (one for each antenna port) must be transmitted through the long fronthaul optical links. The physical layer is responsible to convert the digital bits to radio waves. Fig. 4 reports the downlink stack of radio processing functions in the radio physical layer and most importantly how they can be split between the baseband unit and the radio unit. In classical radio systems (Fig. 4a) all the digital processing is placed inside the baseband and the interface with the RU is via E interface using common public radio interface (CPRI) protocol that is bit rate intensive with a constant bit rate since it transmits raw digitized I/Q samples in the time domain and requires continuous bit transport of multigigabit (even for a single element and a radio BW of only 20 MHz). The bit rate in CPRI scales with both the number of antennas elements and the Radio BW and is independent of traffic since the antenna elements must be active all the time: this makes it not very scalable. New possible functional splits have been defined [13] with the objective to reduce the fronthaul data rate since it would have become unsustainable with massive MIMO and Beamforming and with the wider radio channel bandwidths. Moving up in the stack the fronthaul bit rate decreases since most complex processing functions like beamforming (BF) and inverse fast Fourier transform (iFFT) are moved from baseband unit to radio unit and consequently what it is transmitted

in the fronthaul links are symbols that are traffic related and they require much less bit to be transported [14]. This makes it possible to replace the traditional data intensive CPRI interface with new interfaces named enhanced CPRI (eCPRI) [13] where the amount of data to be transported scales with the actual cell traffic load (i.e., number of occupied OFDM subcarriers) rather than the radio BW and with the number of data streams (named layers) sent to the antenna rather than the number of antenna elements. Considering, as example, the split option point indicated in Fig. 4b the fronthaul throughput requirement is more than an order of magnitude lower with respect to point E [16]. One price to pay for moving the split point up in the stack is a more complex HW implementation of the RU since new digital processing ASICs must be introduced inside it performing some of the Low-PHY functions [14]. In this new RU, the need arises to distribute high speed data across the antenna array between a number of digital processing ASICs performing digital beamforming (DBF) and iFFT functions, and many RFICs. Each RFIC, in turn, is connected to a number of antenna ports (e.g. 8, 16 up to 32). The internal communication interface between ASICs and RFICs is similar to CPRI (E interface in Fig. 4a) and it is a bit rate intensive interface since the RFICs have limited processing power and they can only accomplish basic physical layer functions.

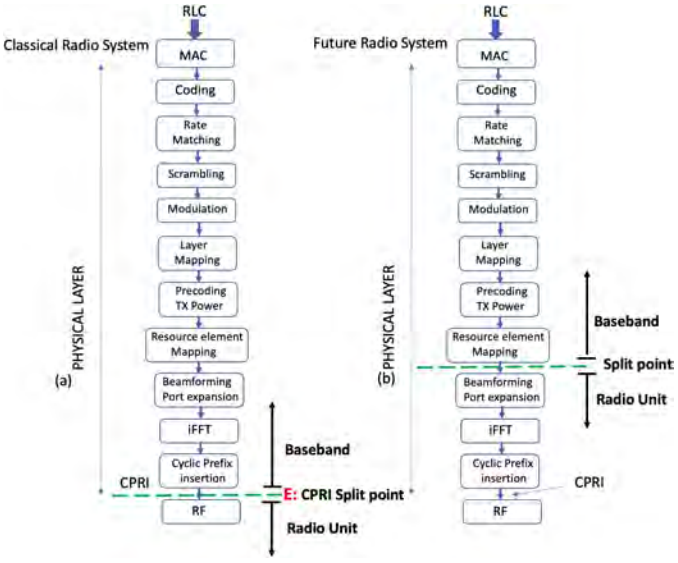


Fig. 4. Radio Physical Layer processing stages and split points: (a) classical radio systems, (b) new radio systems.

A possible hardware architecture of an advanced antenna system (AAS) is shown in Fig. 5. It includes several hundred antenna elements, each one having two antenna ports corresponding to the two cross-polarizations. A number M of digital processing ASICs are placed at the bottom of the antenna box and a number N of RFICs are distributed across the antenna with each RFIC driving a number K of antenna ports in close proximity with RF signals through high-speed copper lines. The ASICs perform the various antenna-centralized digital processing functions included in the Radio Unit and shown in Fig. 4b (beamforming, iFFT, cyclic prefix insertion). The RFICs accomplish the antenna-distributed functions like digital front end (conversion of digital I/Q antenna samples into analog) and the subsequent analog front end (amplification, up and down-conversion etc.). The performances of AAS depend much on the number of antenna elements: the larger is this number, the higher is the effective isotropic radiated power (EIRP) and, consequently, more beams can be simultaneously generated with a higher antenna gain, improving radio coverage and capacity. However, when determining the maximum number of elements in the array we need to consider some limitations like the maximum heat generation inside the antenna, the maximum antenna size and weight and the maximum front-haul bandwidth needed to interconnect such an antenna to the rest of the radio base station. AAS with 64 antenna elements (128 antenna ports) are already commercially available [17] for mid-band systems and in the future it is expected that the number of elements will increase up to 128 (corresponding to 256 antenna ports). In the evolution of 5G, high-band antenna with 512 elements (1024 antenna ports) will be commercially available with a higher gain, required by the increased attenuation, and thanks to the smaller antenna size. Such type of high-band AAS are considered in [18] in which a very recent market outlook of millimeter wave radio products is presented. This trend is expected to continue in 6G systems, made possible by the continuous improvements in power consumption, front-haul bandwidth and by the increase of carrier frequency. High throughput communication between the ASICs and the RFICs occurs via high-speed digital links whose length depends on the carrier frequency. Indeed, the antenna elements in AAS are spaced about a half-wavelength apart and consequently the higher the frequency the smaller is the antenna array size and the shorter are the link lengths. Subdividing the AAS into two categories, sub-6GHz and mmW, we can consider, indicatively, that the maximum link length of a sub-6GHz antenna with 256 antenna ports is of the order of 1 meter while for an mmW antenna with 1024 antenna ports it is a few tens of centimeters.

IV. Requirements

To evaluate possible bottlenecks and to identify key technologies to overcome it, it is important to estimate the total throughput of the communication interface between the ASICs and the RFICs.

The bandwidth requirements of this interface can be roughly calculated with the following formula:

$$B = 2AR_s b_s \tag{1}$$

Where A is the number of antenna ports, R_s represents the sample rate, b_s is the resolution in terms of number of quantized bits per sample and the factor 2 takes into account that I and Q antenna samples are processed separately. In our estimation, we assumed 25% oversampling and 15 bit/sample for the mid-band and 10 bit/sample for high-band systems where the interference environment could be considered more favorable due to smaller distance to terminals and more directive beams. For 6G systems, we assumed 20% oversampling and 10 bit/sample.

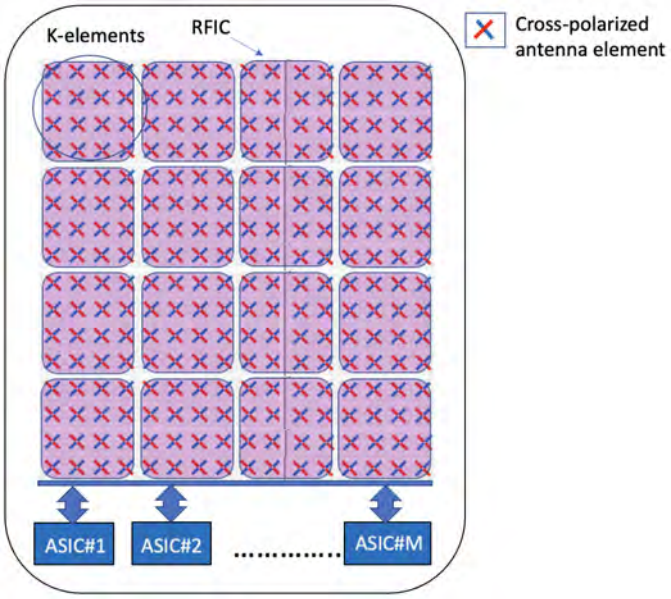


Fig. 5. Hardware architecture of a AAS with 512 antenna ports.

The communication bandwidth estimation is reported in Fig.6 for the three different types of AAS systems in the mid-band (sub-6GHz), high band (mmW) for 5G systems and for 6G systems.

In mid-band the reference configuration is of 400 MHz radio channel bandwidth (corresponding to 500 MS/s sampling rate) and 256 antenna ports. The total required interconnect bandwidth is 3.8 Tbps which can be implemented by a single digital processing ASIC exchanging data with 16 RFICs. The number of antenna ports driven by a single RFIC depends on the maximum length of the PCB lines connecting the RFIC to the antenna ports. With decrease in carrier frequency, the PCB lines become longer, and to reduce the frequency dependent loss in the PCB lines it is assumed that in the mid-band each RFIC drives up to 16 antenna ports.

Each RFIC needs a 240 Gbps data link to exchange data with the ASICs. Today the highest data rate for the electrical I/O of ASICs, fully specified by OIF-CEI [19], is 56 Gbps and packet switch devices using 50 Gbps SERDES are already in production [20].The specifications of electrical I/O at 112 Gbps data rate are currently in progress with five channel reach projects [21], [22], while the implementation of electrical channel at 224 Gbps is still in its infancy with technical discussions started in 2020 [25]and with the target to release a white paper with a body of knowledge. Due to the high frequency dependent loss in the PCB lines the signal bandwidth must be limited to avoid inter-symbol interference (ISI) and PAM8 and PAM 6 modulation formats are selected candidates for electrical data streams $>$ 200 Gbps. However, besides having lower BW, they have also worse SNR with respect to NRZ and PAM-4 and they require a strong FEC to achieve a bit-error-rate $<$ 10-15. The electrical channel length in the PCB for such data rate is limited to about ten centimeters and even for that length complex equalization circuits and dedicated digital signal processing are required reducing significantly the energy efficiency of the link. Additionally, by using many electrical interconnects at ultra-high data rate some other issues must be coped with: increased crosstalk and electro-magnetic interference (EMI) and the implementation of complex PCB and signal routing. For all the above reasons it is desirable to implement optical interconnects in AAS antennas.

In high band systems, operating at mmW frequency 800 MHz radio channel bandwidth and 1024 antenna ports are assumed, leading to a total interconnect bandwidth of 20.5 Tbps. This can be implemented by four 5.1 Tbps digital processing ASICs exchanging data with 32 RFICs, each driving 32 antenna ports. The increase in both the number of antenna ports and of the number of elements controlled by a single RFIC is enabled by the reduced size of the antenna at mmW frequency (element pitch of few millimeters). Each RFIC needs a 640 Gbps interconnect bandwidth to the ASICs that can be implemented with one 160 Gbps optical channel toward each ASICs.

For the AAS of 6G, which will become a reality at the end of this decade, it is assumed that, thanks to the processing capacity scaling according to Moore's law, the ASIC I/O bandwidth will increase up to 24.5 Tbps and that of RFICs to 7.6 Tbps. In 6G the radio channel bandwidth will be increased to 10 GHz (corresponding to 12 GS/s sampling rate) and the maximum number of antenna ports will be set to 2048, leading to a required interconnect bandwidth of 490 Tbps. This antenna can be implemented with 20 digital ASICs of 24.5T bandwidth each connected to 64 RFICs exchanging 380Gbps data with each of the 20 ASICs (7.6 Tbps total RFIC I/O bandwidth). Due to the high number of digital ASICs and the stringent power constraint for the antenna, it will be necessary to disaggregate the ASICs from the antenna panel. Utilizing the distance insensitivity and low latency and bit-error-rate of the optical I/O would enable disaggregation of the ASICs from the antenna array box to facilitate the development of THz band AAS with hundreds of Tbps throughputs without increasing the antenna array power requirements.

	Radio channel BW/ Sample rate	N. Antenna ports	Interconnect BW	HW Implementation
Mid-band AAS	400 MHz/500 MS/s	256	3.8 Tbps	1x3.8T ASIC+16x240G RFICs
High-band AAS	800 MHz/ 1GS/s	1024	20.5 Tbps	4x5.1T ASICs+32x640G RFICs
6G AAS	10 GHz/12 GS/s	2048	490 Tbps	20x24.5T ASICs+64x7.6T RFICs

Fig. 6. AAS interconnect bandwidth requirements

Besides the challenging requirement on interconnect bandwidth there are other important requirements dictated by the particular application in AAS. The target requirements are discussed below.

A. Target Requirements: Energy Efficiency

Heat management is a critical issue in the AAS since the heat transfer mechanism is based on passive cooling. It is assumed that the maximum power consumption in a feasible high band AAS with fully digital beam-forming is in the range of 500-600 W. Increasing power consumption implies generating more heat and requiring a more complex antenna

mechanical design and an increase of weight. By setting the specification that the power consumption of the optical interconnect should be ¡10% of the total AAS power. In a high band 5G AAS of 1024 antenna ports and 800 MHz radio channel bandwidth, the required interconnect bandwidth is about 20.5 Tbps (see Fig.6) and the budget available for the interconnect is 50-60 W resulting in a target energy efficiency of about 2.5-3 pJ/bit. For the 6G AAS, requiring 490 Tbps throughput, even at I/O energies of 1 pJ/bit, just the I/O power would require 490 W, filling the overall power budget. Utilizing optical I/O to disaggregate the ASICs from the antenna array and RFIC could be a viable solution as discussed above.

B. Target Requirements: Latency

In 5G there are some services, like ultra-reliable low latency communication (URLLC), requiring a low end-to-end latency of less than 0.5 ms [24]. It is envisaged that in 6G systems this latency requirement will be even lower for applications of autonomous vehicle, augmented reality and medical imaging [6]. Most of this latency budget is used by packet processing in the core and backhaul networks while it can be assumed that only one tenth is used in the fronthaul fiber link and radio unit resulting in a latency budget of 50μs. This value comprises transmission along the fiber (5μs/km) and the radio unit latency. The latency of optical interconnect inside the antenna should be much lower ($<$ 50ns) to leave almost all this budget available for digital ASICs and RFICs processing. For this reason, PAM-4 modulation and the associated use of FEC should be avoided and it is preferred to use the NRZ modulation format.

C. Target Requirements: Bit Error Rate

Inside the AAS, data should be transferred with high fidelity since, in case of error, no re-transmission is possible and forward error correction is to be avoided not to degrade the latency performance. This implies that the desired BER should be equal or less than 10^{-15} with no FEC.

D. Target Requirements: Temperature Range

The AAS is assumed to operate in a harsh thermal environment without an active cooling. In these conditions the operating temperature inside the antenna box can easily increase to $>$100°C, due to the maximum external temperature with the contribution of power dissipation of the power amplifiers (PA), digital front ends (DFE) and of the digital processing ASICs.

E. Target Requirements: Bandwidth Density

For mid-band AAS the bandwidth density requirement is not critical due to the antenna element pitch in the centimeter range, while for the high band AAS with millimetric pitch this becomes challenging. Assuming that each RFIC controls 32 antenna ports, that is a 4x4 sub-array of cross-polarized elements, at 39 GHz the antenna element pitch (0.6 x wavelength) is about 5 mm and the area occupied by the sub-array is about 20mm x 20mm. The RFIC is under this area and assuming it has 15mmx10 mm size and that there is 1 mm distance between the RFIC chip and the transceiver chip in a multi-chip module, less than 9 mm width are left for the 640 Gbps optical transceiver. The 640 Gbps throughput is subdivided into 4x160Gbps optical links to the ASICs requiring 12 optical fibers (3 fibers per link, transmit data fiber, receive data fiber and external laser fiber) and with a fiber pitch of 250 μm and connector overheads, the room occupied by the fiber array is about 5mm x 3mm (H x W). The photonic chip footprint will be 5mm x 5mm including fiber array landing area and all the opto-electronic circuits should be contained in an area of approximately 5mm x 2 mm resulting in a required bandwidth density of 64 Gbps/mm^2.

In the digital ASIC module, there is more room available since it is not constrained by the fine antenna array pitch, but the interconnect bandwidth is much higher, of 5.1 Tbps subdivided in 32 links of 160Gbps each. The number of required fibers is 96 (32 fibers per link direction and 32 for external laser feeding). Two optical I/O chiplets per ASIC will be able to handle this bandwidth, each with 48 fiber connections, occupying 9mm x 9mm footprint including the area required for the fiber array landing. With 9mm x 6mm area per chiplet for the electronic-photonic circuits, the density of about 47 Gbps/mm^2 is required.

In 6G systems the I/O bandwidth of the RFIC will be scaled up to 7.6 Tbps and also the antenna element pitch will be decreased resulting in a very challenging requirement on the bandwidth density. For an antenna operating with a carrier frequency of 60 GHz (corresponding to a wavelength of 5 mm and a pitch of 3 mm) the 4x4 cross-polarized antenna sub-array occupies an area of about 12mmx12mm. We can assume that the RFIC will shrink to 12mm x 8mm and 12mm x 4mm is the area left for the optical transceiver. The 7.6 Tbps RFIC throughput is subdivided into 20x380 Gbps optical links to the ASICS requiring 60 fibers (20 fibers per direction and 20 fibers to feed the TX from external laser sources). The area occupied by the fiber array is about 10mm x 2mm with a 127 μm array pitch, including the array overhead, and the room left for the optoelectronic circuit is about 12mm x 2mm resulting in a required bandwidth density of 316 Gbps/mm2. On the ASIC side, the required throughput is 24.5 Tbps subdivided into 64 links of 360 Gbps to the RFICs and the number of fibers is 192 (64 per link direction and 64 for TX feeding). Six 8mm x 7mm optical I/O chiplets (three per side) would carry this bandwidth into the ASIC along a 24mm ASIC edge. Taking into account the fiber array connection overheads the area that can be occupied by the electronic-photonic circuits is 8mm x 4mm per chiplet resulting in a required bandwidth density of 127 Gbps/mm^2.

F. Target Requirements: Manufacturability

In this application the cost and volume manufacturability are of paramount importance and respect to the conventional silicon photonics transceivers used in data centers a further step forward is needed. The full compatibility of monolithically integrated electronic-photonic technology with CMOS

fabrication infrastructures is one of the key aspects to exploit the throughput of electronic IC-fab for photonic IC as well, and to share the capacity of the fab. Scalability of electronic-photonic block functionalities is strongly desirable to reduce the development time and cost of photonics transceivers and to facilitate the chip design for specific ASIC requirements. This can be achieved by means of standardization of material, functional blocks and packaging. It is widely recognized that packaging simplification is the top action to be investigated to reduce costs of photonics circuits. Electronic-Photonic integration plays a critical role in the development of low-cost optical interconnects. Monolithic integration of electronics and photonics indeed simplifies the route for packaging with respect to 3D hybrid integration that requires vertical interconnection with through silicon vias (TSV)[23]. Additionally, design for testability is also a crucial aspect in this application and the chip should integrate all the functional blocks allowing autonomous automated testing.

The main optical interconnect requirements are summarized in Fig. 7.

	Interconnect BW	BER	Energy Efficiency	Latency	Shoreline BW density	Area BW density
5G systems	20.5Tbps	$< 10^{-15}$	<2.5-3 pJ/bit	<50 ns	RFIC: 128Gbps/mm ASIC: 283Gbps/mm	RFIC: 64 Gbps/mm^2 ASIC: 47 Gbps/mm^2
6G systems	490 Tbps	$< 10^{-15}$	<1-2 pJ/bit	<50 ns	RFIC: 633 Gbps/mm ASIC: 510 Gbps/mm	RFIC: 316 Gbps/ mm^2 ASIC: 127 Gbps/ mm^2

Fig. 7. Optical Interconnect Requirements.

V. Technologies

In this section, we present recent progress in a new generation of co-packaged optical I/O technologies that lead to increased energy efficiency, bandwidth density, and lower link latencies. The optical I/O technology was built from the ground up to address the electrical I/O bandwidth-distance bottleneck that has created a "power wall" for continued ASICs performance scaling. As we will show in this section, this technology has the capability to answer the requirements metrics of the future systems laid-out in the previous section.

Figure 8 shows the key elements of the core technology stack. First, as shown in Fig. 8(a), an optical device technology is chosen that is small enough to allow dense, energy-efficient electrical systems to be built on top of it. Furthermore, this device technology must be compatible with existing high-volume CMOS foundry infrastructure while requiring minimal process changes. This allows the technology to leverage previous industry investments in CMOS foundries and assembly, test, and packaging technologies that already exist for high-volume applications. To satisfy these constraints, we choose silicon microring technology for the following reasons:

1) Silicon microrings are small ($\approx 10\,\mu$m diameter) and can operate at high speeds ($25 - 100$ Gbps). This satisfies the density and energy efficiency requirements for the core devices.There is a relation between microring size, energy efficiency and modulation bandwidth. The smaller is the microring radius, the higher is the energy efficiency due to the smaller capacitance to be driven by the electrical driver. Conversely, the phase accumulated per round trip is proportional to the ring radius and smaller microrings need higher Q in order to get the required phase shift for modulation. However, the higher the Q,the smaller is the modulation bandwidth due to longer photon lifetime. Therefore, the right trade-off between energy efficiency and bandwidth must be found.
2) Silicon microrings can be readily manufactured in existing SOI CMOS processes using 193 nm immersion lithography and standard doping recipes to create p/n junctions for electrical control of the microrings.
3) Silicon microrings are a natural fit for wavelength division multiplexing (WDM) which allows large aggregate bandwidths (0.1 to 1 Tbps) to be aggregated on a single fiber.
4) Silicon microring resonances can be locked to laser wavelengths by means of low power circuits controlling the currents of micro-heaters, placed on top of the microrings. This allows the use of uncooled WDM lasers avoiding laser wavelength stabilization with power hungry thermo-electric coolers.

Monolithic integration, as shown in Fig. 8(b), allows all of the electrical circuitry (TIAs, drivers, digital control, equalization, etc.) to be densely integrated on the same die as the photonic devices (waveguides, microring modulators, microring filters, photodetectors, etc.). A single die solution, Fig. 8(c), simplifies the packaging requirements, and allows for the die to intercept the latest "chiplet" packaging and assembly techniques offered by high-volume OSATs as shown in Fig. 8(d).

Figure 9 shows a simplified schematic of the TeraPHY WDM optical I/O architecture. The TeraPHY optical I/O chiplet is co-packaged with a host SoC and communicates to the SoC through an electrical interface. Since the TeraPHY chiplet is a single CMOS chiplet and can operate at high temperatures, it can be integrated very closely to the host SoC (< 1 mm) to minimize the distance that the electrical signals need to propagate before electrical-to-optical conversion. An important feature of this architecture is the disaggregation of the laser source. The SuperNova laser source is a multi-wavelength, multi-port laser that supplies all of the WDM continuous wave laser power to the TeraPHY chiplet. By disaggregating the laser source from the optical Tx/Rx, the lasers can be managed in a separate thermal environment to improve reliability and field replaceability. Once the data is encoded optically, single-mode fibers carry data to and from TeraPHY chiplets. This allows a large span of physical distances to be traversed. Whether transmitting data between sockets on the same board (≈ 10 cm) or across a datacenter (≈ 2 km), or between the RU panel and the baseband processing station, the same TeraPHY chiplet is used without need for amplification between Tx/Rx.

Figure 10 shows the main pieces of the TeraPHY chiplet architecture. At the bottom of the chip, an electrical interface brings electrical data into the chip. The electrical data is then converted to the optical domain through the optical macros. The optical macros are an array of optical Tx/Rx that

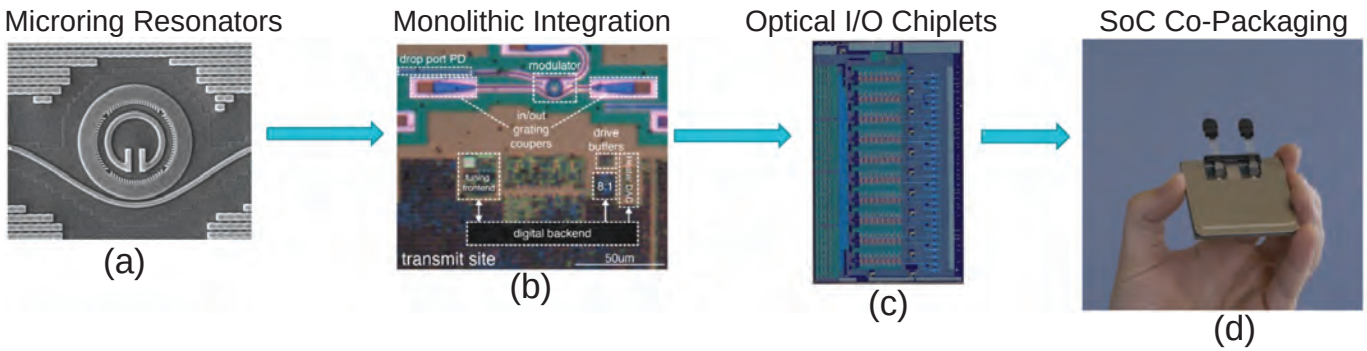


Fig. 8. Key elements of the TeraPHY chiplet technology.

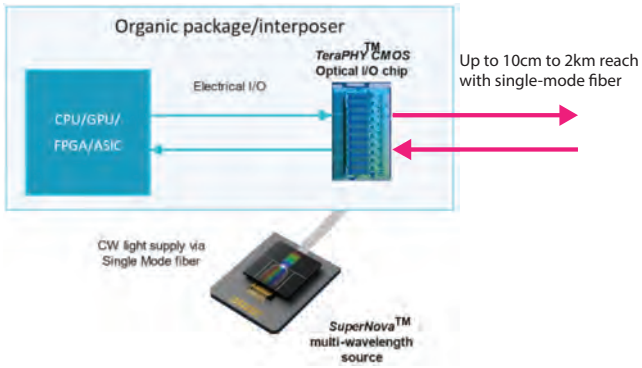


Fig. 9. Optical I/O architecture.

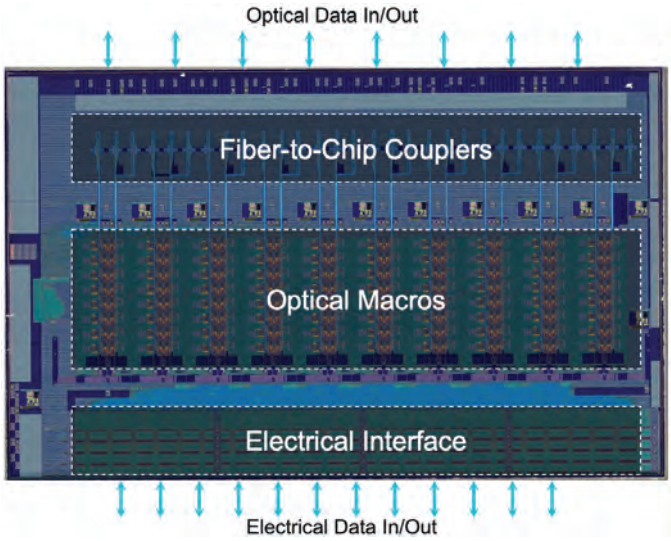


Fig. 10. TeraPHY chiplet architecture.

contain all of the electrical circuitry and the photonic devices required for optical I/O (serializers, deserializers, modulator drivers and transimpedance amplifiers, clocking subsystems, ring resonance control logic etc). Optically encoded data is coupled into and out of the chip through an array of chip-to-fiber couplers shown at the top of the chip. This design was chosen to be modular in its ability to mix and match electrical interfaces with the optical macros without requiring changes to the optical macro or optical coupler array designs. The optical macros are comprised of an array of WDM macros with cascaded microring resonator devices. In each macro, the optical transmitters use each microring modulator as an independent communications channel. The optical receivers use microring devices as WDM demultiplexers that select optically encoded data on particular optical frequencies and redirect those optical frequencies to photodetectors for optical-to-electrical conversion and follow-on receiver electronics. Current TeraPHY prototypes are built with eight optical Tx/Rx macros each with eight microrings per macro such that the chiplet is an 8-port$\times$8-λ/port device. This results in 64 independent optical channels that can be used for optical I/O. The TeraPHY prototype chiplet size is 5.5mm x 9mm.

Figure 11 shows a summary of measured data from the TeraPHY prototype chiplet [27]. Figure 11(a) shows passive (untuned) relative insertion loss through all eight ports of the transmitter path (laser input, transmitter output). The resonances of all eight microrings can be seen, and the wavelength range plotted is larger than the free-spectral range (FSR) of the devices such that more than eight resonances appear. In aggregate, there are 128 microrings on the TeraPHY chiplet that are used in full-duplex communications (eight ports with eight Tx microrings per port and eight Rx microrings per port). Each microring has a slightly different diameter such that the designed resonance frequencies fall on a grid. This is done so that on average, each individual microring only needs to thermally tune $\approx$ 1 to 2 channel spacings to lock on to the incoming laser frequencies, thus minimizing the required thermal tuning power. We previously demonstrated excellent thermal tuning efficiencies in microring devices [26].

Figures 11(b),(c) summarize single wavelength characterization at both 16 Gbps/λ and 25 Gbps/λ. The TeraPHY chiplet was designed to be configurable between 16 to 25 Gbps/λ. On-chip pseudo-random bit sequence generators are used to transmit random data and characterize the transmitter optical eye diagrams and the received statistical eye diagrams. The 25 Gbps Rx statistical eye diagram is shown post decision feedback equalization (DFE) using the Rx built-in bit-error-rate checking electronics. The pie charts report measured energy efficiencies of the optical macros. The measurement was conducted by measuring the current drawn by the voltage rails, calculating power ($P = V \times I$), and dividing by the data

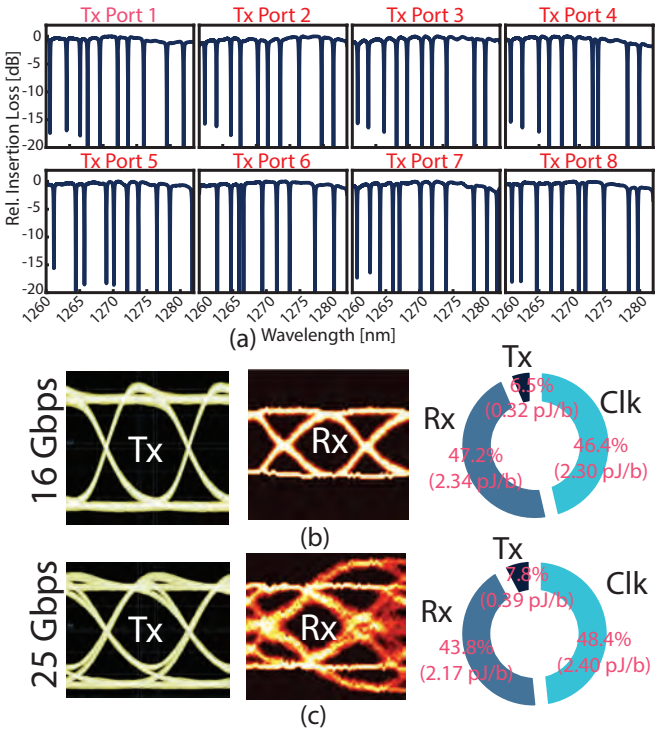


Fig. 11. TeraPHY chiplet data.

rate. The measured energy efficiency of the optical macros is 4.96 pJ/bit for both 16 Gbps and 25 Gbps operation. The majority of the power is consumed in the high-speed clock generation and distribution (phase-locked loops, phase interpolators, clock buffers, etc.) and the receiver (transimpedance amplifiers, CTLE, DFE, CDR, etc.). We expect significant improvements in energy efficiency in follow-on designs that further optimize the electrical circuitry. 1 to 2 pJ/bit for the optical macros is feasible through optimization, and < 1 pJ/bit is possible using future R&D concepts that we have developed.

Next, we present details on the SuperNova laser module. The basic architecture is presented in Fig. 12(a). An array of M DFB lasers couple into a passive $M \times N$ multiplexer and splitter to create an output array of N output optical ports that connect to single-mode fibers with each output optical port carrying M wavelengths of light. This architecture allows a scalable approach to increase the number of wavelengths and output ports.

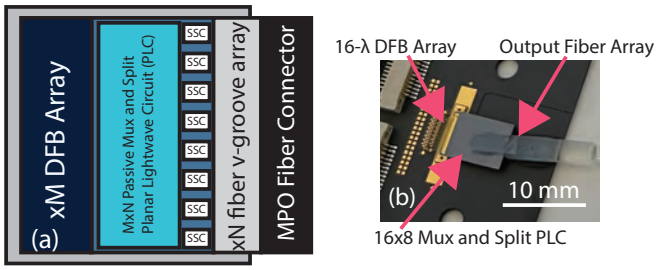
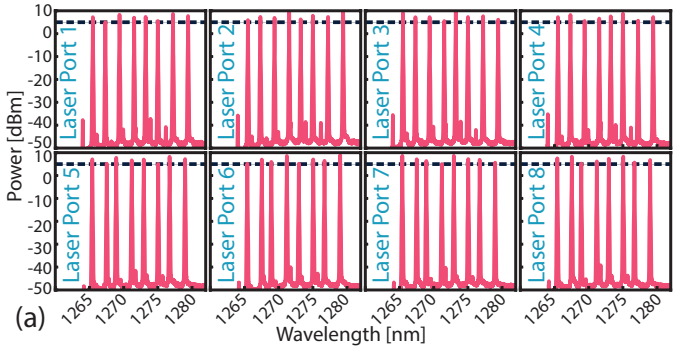


Fig. 12. (a) SuperNova laser module architecture. (b) SuperNova prototype in the 16x8 configuration.

Figure 12(b) shows an assembled SuperNova prototype using a 16-λ DFB laser array and a 16×8 multiplexer and splitter implemented using a planar lightwave circuit (PLC) [27]. The output of the DFB array is butt-coupled to the input of the PLC. The PLC contains two 8x8 passive multiplexers and spot-size converters (SSC) that are used to expand the optical mode profile for efficient coupling to single-mode fibers. The sub-components are assembled onto a ceramic package substrate, and wirebonds supply electrical current to the DFB array.



(b)

λ (nm)	1265.5	1267.3	1269.4	1271.5	1273.2	1275.0	1277.2	1279.4
Port 1 (mW)	5.3	3.2	6.7	5.0	5.4	3.6	7.3	5.9
Port 2 (mW)	3.9	5.4	4.9	8.5	4.2	6.1	5.4	9.9
Port 3 (mW)	8.1	5.2	5.3	3.6	8.7	5.3	5.8	4.1
Port 4 (mW)	5.3	6.6	3.6	4.6	5.7	7.4	3.7	5.3

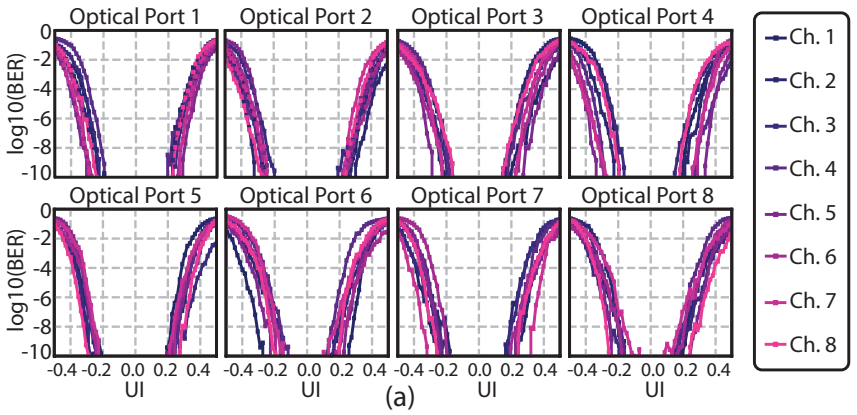
λ (nm)	1265.4	1267.5	1268.9	1271.2	1273.0	1275.1	1276.7	1279.0
Port 5 (mW)	5.1	3.3	6.0	4.6	5.0	3.2	6.6	5.2
Port 6 (mW)	3.3	5.0	4.0	7.2	3.3	5.1	4.4	7.8
Port 7 (mW)	7.3	5.2	4.3	3.2	7.3	5.3	4.9	3.7
Port 8 (mW)	5.6	6.7	3.3	4.1	5.4	6.7	3.7	4.8

Fig. 13. SuperNova laser module architecture.

Figure 13 presents characterization data of the SuperNova module. Measured optical spectra from every output port of the SuperNova module are shown in Fig. 13(a), and power per wavelength and center wavelength are shown in Fig. 13(b). Most SuperNova ports have $\approx$ 2-4 dB of power imbalance between the wavelength with the minimum power and the wavelength with the maximum power.

Finally, we present the full characterization of the TeraPHY optical I/O architecture [27]. Figure 14a illustrates the BER bathtub curves for a full link demonstration of 1.024 Tbps between the two TeraPHY chiplets, while Fig. 14b shows the total data transmitted per port during the experiment, with zero errors recorded per port.

Referring back to the optical interconnect requirements laid-out in Fig. 7, the prototype TeraPHY chiplet achieves 113-177 Gbps/mm shoreline bandwidth density depending on the mode of operation and area bandwidth densities of $20 - 32$ Gbps/mm^2. Including the electrical interface energy of 1 pJ/bit, the whole chiplet consumes 6 pJ/bit, while having



Optical Port #	Total Bits Sent/Received	Errors
1	14.386 Terabits	0
2	15.106 Terabits	0
3	11.675 Terabits	0
4	14.106 Terabits	0
5	14.502 Terabits	0
6	10.488 Terabits	0
7	13.585 Terabits	0
8	10.317 Terabits	0

(b)

Fig. 14. (a) Full link demonstration of 1.024 Tbps between the two TeraPHY chiplets with bathtub BER curves shown for each channel of every port. (b) Total data transmitted per port during the experiment, with zero errors recorded per port.

the latency under 10 ns and achieving better than 10^{-15} BER. These metrics are already very close to meeting the 5G system requirements and with production chiplet throughputs starting at 2 Tbps and doubling in every generation, and energy-efficiencies improving through further design optimization TeraPHY chiplet technology has a clear path to addressing the needs of future 6G systems.

VI. Conclusions

In this paper we analyze the architectures for future advanced antenna array systems and develop the interconnect metrics required to meet the needs of these future systems. From these, it is clear that traditional electrical interconnect technologies cannot meet the energy-efficiency, reach, bandwidth-density, latency and bit-error rate requirements. To overcome these limitations we propose the use of the emerging optical I/O technology and develop the required metrics and architectures for the optical I/O for antenna array systems. The experimental results of the TeraPHY optical I/O prototype and its design features confirm that this technology has a clear path to address the system challenge of the future antenna array systems.

VII. Acknowledgment

We would like to thank Dr. Filippo Ponzini at Ericsson Research in Pisa for helpful discussions.

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